ECR #: 17
Title: Clarification of section 6.1.2.
Release Date: Feb. 10, 1997
Impact: Clarification
Spec Version: A.G.P. 1.0

Summary: Re-write section 6.1.2. to improve clarity about traffic between the different ports (Host Bus, A.G.P., primary PCI bus segments and Main memory). (This also reflects changes made with ECR-16.)

Background: Original text was confusing about the interaction between the different ports. This ECR clarifies what transactions are supported between the different ports.

Change Current Specification as shown:

Replace existing Section 6.1.2. with the following text.

Section 6.1.2.

A.G.P. Compliant Target Devices

A typical host bus bridge (also known as corelogic) is illustrated in Figure 0-1. The host bus provides a port to the Processor, System Memory, the PCI bus and to A.G.P.. The area inside the dotted line represents the A.G.P. compliant target or corelogic. The blocks inside the dotted line represent different functions that the host bridge usually provides. The following paragraphs will describe which accesses are supported at each port and may depend on the destination of the request whether it is supported or not. The arrows in the figure describe paths in which transactions are routed inside the corelogic. Each port will be discussed and the associated paths (arrows) will be described.

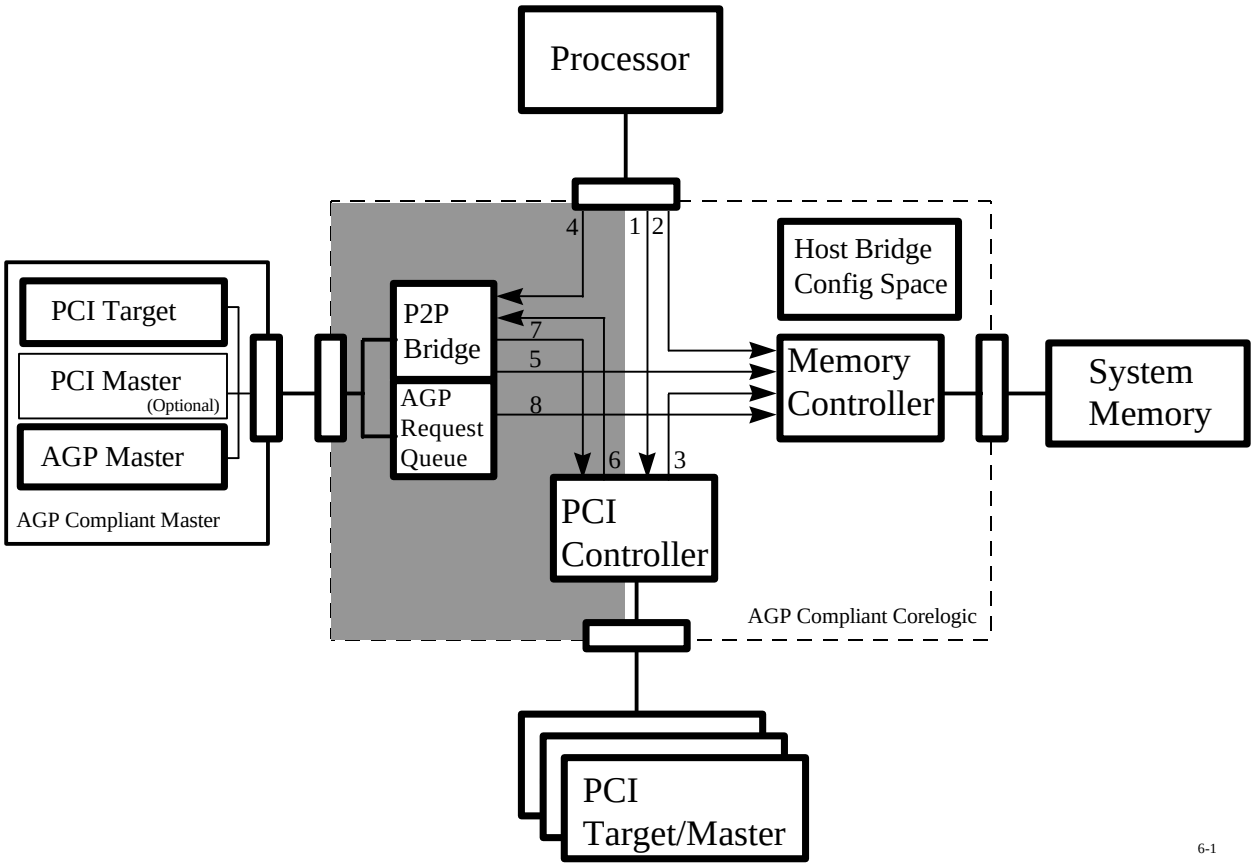

Figure 0-1 Configuration View of an A.G.P. Target

Corelogic Ports

Processor Port

The processor port provides a means for the processor to generate accesses to the PCI controller (path 1), to the P2P (PCI to PCI Bridge) (path 4) and to the Memory Controller (path 2). The corelogic determines to which port these accesses are routed by using information stored in Host Bus Bridge Config Space block. This information is provided during the initiation process.

System Memory Port

This port provides a means to connect System Memory to the corelogic. The Memory Controller is responsible for converting accesses that are initiated on other ports (Processor, A.G.P. and PCI) into memory commands.

PCI Port

The PCI Controller converts processor accesses into PCI transactions. Since the processor has no Configuration commands, the PCI Controller generates PCI Configuration commands as described in the PCI Local Bus specification. The PCI controller takes memory commands that address system memory and forwards them to the Memory Controller (path 3). The PCI Controller also provides a means for PCI masters to access the PCI target that resides on the A.G.P. port and is represented by path 6 in the shaded area. This path is limited in its functionality and the corelogic is not required to provide full PCI to PCI bridge functionality. The corelogic

provides support for PCI write[1] commands as described in the PCI specification, while support of other PCI commands is optional.

A.G.P. Port

When the corelogic supports an A.G.P. port it requires new logic that has not been incorporated in previous chipsets, however no new functionality is required to boot the system. This new logic is shown in Figure 0-1 as a shaded area. To enable the use of existing enumeration code (unmodified) to handle A.G.P. compliant devices the corelogic will use functionality already defined by the PCI Local Bus Specification. The P2P Bridge block facilitates the configuration of the second I/O port (A.G.P.) of the corelogic using compliant enumeration code and follows the PCI to PCI Bridge Architecture Specification. The P2P bridge makes it possible to configure the PCI target interface in an A.G.P. compliant master device. This information is also used to route memory and I/O addresses to the PCI target of a A.G.P. compliant master from the processor. The P2P bridge block is not required to be a fully functioning PCI to PCI Bridge. The corelogic is only required to support PCI write commands from the PCI to the A.G.P. port. The corelogic may optionally support other PCI commands between PCI and A.G.P. or A.G.P. and PCI but there is no requirement. The processor can initiate transactions to a PCI target on the A.G.P. port by path 4. Path 7 optionally provides a path for the A.G.P. compliant master using PCI protocol to access a target on PCI. The A.G.P. compliant master can initiate PCI commands to the memory controller by path 5. Path 5 and path 3 have the same capabilities. The new functionality provided by the A.G.P. port is represented by the A.G.P. Request Queue block. This block accepts A.G.P. commands from the A.G.P. compliant master. Once A.G.P. commands are accepted by the request queue, it is implementation specific how these requests are presented to the Memory Controller and is illustrated by path 8. The A.G.P. compliant master doing A.G.P. commands can only access system memory. Support to any other port is not required or supported by this specification.

The A.G.P. Compliant Master (Solid line around the A.G.P. Compliant Master, PCI Master and PCI Target blocks also identified as a AGP Compliant Master) is allowed to initiate any A.G.P. commands described in section 3.1.2.. The PCI Master is allowed to initiate any PCI command specified in the PCI Local Bus Specification. Which commands the corelogic is required to support and which commands may be optionally supported are listed in Table 0-1. How the corelogic behaves when an unsupported command is used is not defined by this specification[2].

Table 0-1 Commands Supported by Each Port

Path	Commands Required to be Support by Corelogic	Commands Optionally Supported by Corelogic
1	Processor memory read and write, I/O read and write, corelogic generates PCI Configuration Read and Write commands from Processor I/O read and write commands per PCI 2.1.	Interrupt Acknowledge, CPU Special Cycles
2	Processor memory read and write commands.	N/A
3	Memory Read, Memory Read Line, Memory Read Multiple, Memory Write, and Memory Write and Invalidate	I/O (read and write) and Configuration (read and write)
4	Same as 1.	N/A
5	Same as 3	N/A
6	Memory Write and Memory Write and Invalidate	I/O (read and write), Configuration (read and write) and memory read (Read, Read Line and Read Multiple)
7	No support required.	I/O (read and write), Configuration (read and write), memory read (Read, Read Line and Read Multiple) and memory write (Write and Invalidate, and Write).

[1] Memory Write and Memory Write and Invalidate commands.

[2] Chipset can ignore the request and allow it to be terminated with Master Abort or claim the access and return FFFF FFFFh on a read and drop write data by asserting TRDY#.

8	A.G.P. Commands	N/A

The Host Bridge Config Space block contains configuration registers used to specify parameters associated with the Graphics Address Remapping Table (*GART*) and circuitry in the A.G.P. interface. The corelogic uses a PCI base address register to request a naturally aligned block of memory address space in which to locate the GART address range. Initiation code determines the size requested and allocates the resource. The bridge also uses this information to route requests initiated by the processor to either the Memory Controller, PCI Controller or P2P Bridge.